CLAIMS

What is claimed is:

1. A computer data signal embedded in one of a machine readable device and a machine readable medium comprising:
   a first code group having a first symbol and an error detection code for the first symbol; and
   a second code group having a second symbol different from the first symbol and an error correction code for a third symbol that includes the first symbol and the second symbol.

2. The computer data signal of claim 1 wherein the third symbol further includes the error detection code.

3. The computer data signal of claim 1 wherein the computer data signal further comprises a plurality of second code groups, each of said plurality of second code groups containing one of a plurality of second number of bits and one of a plurality of sets of error correction bits for the first number of bits and the one of the plurality of second number of bits.

4. The computer data signal of claim 1 wherein the error correction code provides error correction information for the first symbol if the error detection code indicates an error, and error correction information for the second symbol otherwise.

5. The computer data signal of claim 1 wherein the error detection code is a parity bit.

6. The computer data signal of claim 1 wherein the error detection code is a plurality of parity bits, where each of said plurality of parity bits can detect an error in a predetermined portion of the first symbol.

7. A method for transmitting correctable data comprising:
   receiving information data having a first symbol and a second symbol different from the first symbol;

generating error detection data for the first symbol;
transmitting the first symbol and the error detection data;
generating error correction data for the first symbol and the second symbol; and

transmitting the second symbol and the error correction data.

8. The method of claim 7 wherein generating error correction data further comprises generating error correction data for the error detection data.

9. The method of claim 7 wherein the information data is further comprised of a plurality of second symbols, and the method further comprises generating error correction data for the first symbol and one of the plurality of second symbols, and transmitting said one of the plurality of second symbols and said error correction data.

10. The method of claim 7 wherein the error correction data includes the error detection data.

11. A method for receiving correctable data comprising:
receiving a first transmitted code group having a first information symbol and error detection data for the first transmitted code group;
detecting an error in the first transmitted code group;
if the error is not detected
providing the first information symbol as a first valid information symbol;
otherwise
receiving a second transmitted code group having a second information symbol different from the first information symbol and error correction data for the first information symbol and the second transmitted code group,
performing error correction on the first and second information symbols, and
providing the first information symbol as the first valid information symbol after performing error correction.

12. The method of claim 11 wherein performing error correction includes performing error correction on the error detection data.

13. The method of claim 11 wherein receiving the second transmitted code group further comprises receiving one of a plurality of second transmitted code groups, each of said plurality of second transmitted code groups comprised of one of a plurality of second information symbols and one of a plurality of error correction data for said first information symbol and said one of a plurality of second transmitted code groups.

14. The method of claim 11 wherein the error correction data includes the error detection data.

15. A data transmission device comprising:
a first register that receives a first number of bits;
a second register that receives a second number of bits different from the first number of bits;
an error detection generator coupled to the first register that generates an error detection bit for the first number of bits;
an error correction generator coupled to the first register and the second register that generates a set of error correction bits for the first number of bits and the second number of bits;
a first data transmitter coupled to the first register and the error detection generator that transmits the first number of bits and the error detection bit; and
a second data transmitter coupled to the second register and the error correction generator that transmits the second number of bits and the set of error correction bits.

16. The data transmission device of claim 15 wherein the error correction generator generates the set of error correction bits for the first number of bits, the second number of bits, and the error detection bit.

17. The data transmission device of claim 15 further comprising:

a plurality of second registers that receives one of a like plurality of the second number of bits;

a like plurality of error correction generators, coupled to the first register and one of said plurality of second registers, each of said plurality of error correction generators generating a set of error correction bits for the first number of bits and one of said plurality of the second number of bits; and

a like plurality of second data transmitters coupled to one of said plurality of second registers and one of said plurality of error correction generators to transmits one of said plurality of second number of bits and said set of error correction bits.

18. The data transmission device of claim 15 wherein the error correction generator is further coupled to the error detection generator and the set of error correction bits includes the error detection bit.

19. An data reception device comprising:

a first register that receives a first number of bits and an error detection bit for the first number of bits;

a first data available indicator;

an error detector coupled to the first register and the first data available indicator, said error detector to detect a first error in the first number of bits and to set the first data available indicator if the first error is not detected;

a second register that receives a second number of bits different from the first number of bits and a plurality of error correction bits for the first number of bits and the second number of bits;

a second data available indicator; and

an error corrector coupled to the first register, the second register, the first data available indicator, and the second data available indicator, said error corrector to correct a second error in the first number of bits and the second number of bits, and to set the first and second data available indicators.

20. The data reception device of claim 19 wherein said error corrector further corrects the second error in the first number of bits, the second number of bits, and the error detection bit.

21. The data reception device of claim 19 wherein the error corrector further corrects one of the first error in the first number of bits, the second error in the second number of bits, and the second error in the error detection bit.

22. A computer data signal embedded in one of a machine readable device and a machine readable medium comprising:

a first code group having a first symbol and a first code for the first symbol, the first code providing a first level of error protection for the first symbol; and

a second code group that is transmitted after the first code group, the second code group having a second symbol different from the first symbol and a second code, the second code providing a second level of error protection for a third symbol that includes the first symbol and the second symbol, the second level of error protection being greater than the first level of error protection.

23. The computer data signal of claim 22 wherein the first code is a single bit error detection code and the second code is an error correction code.

24. The computer data signal of claim 22 wherein the third symbol further includes the error detection code.